## CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A logic circuit including:

A plurality of look up tables ("LUTs") driven by a plurality of inputs, each of the plurality of LUTs included either in a first group of LUTs or a second group of LUTs;

at least one of the plurality of inputs driving each of the plurality of LUTs;

at least a second of the plurality of inputs driving each LUT in the first group of LUTs and connectable to drive at least one of the LUTs in the second group of LUTs;

at least a third of the plurality of inputs connectable to drive at least one of the LUTs in the first group of LUTs;

at least two LUTs in the first group of LUTs each driving a first multiplexer ("MUX") and a second MUX; and

at least a fourth of the plurality of inputs driving a control input of the first MUX.

2. The logic circuit of claim 1 including:

at least a fifth input driving each LUT in the second group of LUTs and connectable to drive at least one of the LUTs in the first group of LUTs;

at least a sixth input of the plurality of inputs connectable to drive at least one of the LUTs in the second group of LUTs;

at least two LUTs in the second group of LUTs each driving a third MUX and a fourth MUX; and

at least a seventh input of the plurality of inputs driving a control input of the third MUX.

3. The logic circuit of claim 2 including a first input MUX and second input MUX the first input MUX driven by the at least third input and the at least fifth input wherein the first input MUX drives at least one of the LUTs in the first group of LUTs and the control input of the second MUX and the second input MUX drives at least one of the LUTs in the second group of LUTS and the control input of the fourth MUX.

4. The logic circuit of claim 3 wherein:

one of the LUTs of the first group of LUTs drives a first output MUX and one of the LUTs of the second group of LUTS drives the first output MUX;

the second MUX drives a second output MUX and the fourth MUX drives the second output MUX; and

the first output MUX and second output MUX both drive a third output MUX.

5. The logic circuit of claim 4 wherein:

one of the LUTs of the first group of LUTs drives a fourth output MUX and one of the LUTs of the second group of LUTS drives the fourth output MUX;

the fourth MUX drives a fifth output MUX and the second MUX drives the fifth output MUX; and

the fourth output MUX and fifth output MUX drive a sixth output MUX.

6. The logic circuit of claim 5 wherein a control input of the third output MUX is driven by the at least fourth of the plurality of inputs and a control input of the sixth output MUX is driven by the at least seventh of the plurality of inputs.

7. The logic circuit of claim 6 including a first adder and a second adder wherein:

the first adder is driven by one of the plurality of LUTs in the first group of LUTs and a first adder MUX, wherein the first adder MUX is driven by the first MUX and a share input to the logic circuit; and

the second adder is driven by one of the plurality of LUTs in the second group of LUTs and a second adder MUX, where the second adder MUX is driven by the second MUX and the third MUX.

8. The logic circuit of claim 7 wherein the first adder is further driven by a carry-in input to the logic circuit and the second adder is further driven by a carry-out output of the first adder and drives a carry-out signal of the logic circuit.

9. The logic circuit of claim 8 including a first register portion and a second register portion, the first register portion including a first register which can be interconnected with one of either an output of the first adder and an output of the third output MUX, the second register portion including a second register which can be interconnected with one of either an output of the second adder and an output of the sixth output MUX.

10. The logic circuit of claim 9 wherein the first register can be interconnected with a register cascade input to the logic circuit and the second register can be interconnected with an output of the first register.

11. The logic circuit of claim 10 wherein the first input MUX is further driven by the output of the first register and the second input MUX is further driven by an output of the second register.

12. The logic circuit of claim 11 including a first set of final output MUXs and a second set of final output MUXs wherein:

each MUX of the first set of final output MUXs is driven by an output of the first adder, the output of the first register and the output of the third output MUX; and

each MUX of the second set of final output MUXs is driven by an output of the first adder, an output of the second register and the output of the sixth output MUX.

13. The logic circuit of claim 9 including a first sharing MUX driving the control input of the first output MUX and a second sharing MUX driving the control input of the fourth output MUX wherein:

the first sharing MUX is driven by the at least third input and a ground signal; and

the second sharing MUX is driven by the at least sixth input and a control voltage signal.

14. The logic circuit of claim 13 wherein the first sharing MUX is further driven by an output of the first register; and

the second sharing MUX is further driven by an output of the second register.

15. The logic circuit of claim 1 wherein:

the first group of LUTs includes a 4-input LUT and two 3-input LUTs; and

the second group of LUTs includes a 4-input LUT and two 3-input LUTs.

16. A logic circuit including:

a plurality of inputs;

a first plurality of look-up tables ("LUTs") which can be driven by at least a first portion of the inputs and a second plurality of LUTs which can be driven by at least a second portion of the inputs;

a first plurality of multplexers ("MUXs") which can be driven by at least a portion of the first plurality of LUTs and a second plurality of MUXs which can be driven by at least a portion of the second plurality of LUTs;

at least a first adder and a second adder wherein:

the first adder is driven by one of the first plurality of LUTs and at least one of either:

one of the first plurality of multiplexers; and

a share-in input to the logic circuit;

the second adder is driven by one of the second plurality of LUTs and one of either:

one of the second plurality of multiplexers; and

one of the first plurality of multiplexers.

17. The logic circuit of claim 16 that can be interchangeably configured in one of at least a first configuration and a second configuration,

the first configuration carrying out a first 6-input logic function along with a second 6-input logic function, the first 6-input logic function sharing at least 4 inputs with the second 6-input logic function; and

the second configuration carrying out a first 5-input logic function along with a second 5-input logic function, the first 5-input logic function sharing at least 2 inputs with the second 5-input logic function.

18. The logic circuit of claim 17 that can be configured in a third configuration interchangeably with the first configuration and the second configuration, the third configuration carrying out a first 4-input logic function along with a second 4-input logic function wherein the first 4-input logic function shares no inputs with the second 4-input logic function.

19. The logic circuit of claim 18 that can also be configured in a fourth configuration interchangeably with the first configuration, second configuration and third configuration, the fourth configuration carrying out a 7-input logic function.

20. The logic circuit of claim 17 including a first register and a second register wherein:

the first register can be driven by either of:

one of the first plurality of MUXs; and

an output of the first adder;

the second register can be driven by either of:

one of the second plurality of MUXs; and

an output of the second adder.

21. The logic circuit of claim 18 wherein:

the first register can also be driven by a register cascade input to the logic circuit; and

the second register can also be driven by an output of the first register.

22. The logic circuit of claim 18 wherein:

an output of the first register can drive at least one of the first plurality of LUTs; and

an output of the second register can drive at least one of the second plurality of LUTs.

23. A logic circuit including:

a plurality of inputs;

a first plurality of look-up tables ("LUTs") which can be driven by at least a first portion of the inputs and a second plurality of LUTs which can be driven by at least a second portion of the inputs; and

a first plurality of multplexers ("MUXs") which can be driven by at least a portion of the first plurality of LUTs and a second plurality of MUXs which can be driven by at least a portion of the second plurality of LUTs; wherein the logic circuit can be interchangeably configured in one of at least a first configuration, second configuration and third configuration,

the first configuration carrying out a first 6-input logic function along with a second 6-input logic function, the first 6-input logic function sharing at least 4 inputs with the second 6-input logic function;

the second configuration carrying out a first 5-input logic function along with a second 5-input logic function, the first 5-input logic function sharing at least 2 inputs with the second 5-input logic function;

the third configuration carrying out a first 4-input logic function along with a second 4-input logic function wherein the first 4-input logic function shares no inputs with the second 4-input logic function.

24. The logic circuit of claim 23 that can also be configured in a fourth configuration interchangeably with the first configuration, second configuration and third configuration, the fourth configuration carrying out a 7-input logic function.